



Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT****Complete if Known**

Application No.	10/733,153
Filing Date	December 10, 2003
First Named Inventor	Donald E. Steiss
Art Unit	2181
Examiner Name	William M. Treat
Attorney Docket Number	22347-08260 (Seq. No. 8116)

Sheet	1	of	1
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**U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document No. Number - Kind Code <sup>2</sup> (if known)	Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
WMT	A1	US-5,881,277	03-09-1999	Bondi et al.
	A2	US-5,991,792	11-23-1999	Nageswaran
	A3	US-6,785,890	08-31-2004	Kalafatis et al.
	A4	US-6,792,446	09-14-2004	Merchant et al.
	A5	US-6,889,319	05-03-2005	Rodgers et al.
	A6	US-7,051,329	05-23-2006	Boggs et al.
	A7	US-2003/0037228	02-20-2003	Kelsey et al.
	A8	US-2003/0163675	08-28-2003	Bennett et al.
WMT	A9	US- 2003/0163589	08-28-2003	Bunce et al.

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document Country Code <sup>3</sup> - Number <sup>4</sup> Kind Code <sup>5</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T <sup>6</sup>

**OTHER REFERENCES - NON-PATENT LITERATURE DOCUMENTS**

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Examiner Signature	W. TREAT	Date Considered	3/3/07
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22347/08260/DOCS/1658173.1



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## **U.S. PATENT DOCUMENTS**

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WMT		US-5,613,114	03-18-1997	Anderson et al.
		US-5,724,586	03-03-1998	Edler et al.
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		US-6,073,159	06-06-2000	Emer et al.
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		US-6,308,261	10-23-2001	Morris et al.
		US-6,341,347	01-22-2002	Joy et al.
		US-6,353,881	05-05-2002	Chaudhry et al.
		US-6,385,715	05-07-2002	Merchant et al.
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22347/08260/DOCS/1412274.1

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WMT		US-6,507,862	01-14-2003	Joy et al.
		US-6,535,905	03-18-2003	Kalafatis et al.
		US-6,542,920	04-01-2003	Belkin et al.
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WMT	C2	Boothe, B. and Ranade, A. G., "Improved Multithreading Techniques for Hiding Communication Latency in Multiprocessors," ACM 1992, pp. 214-223.		

Examiner Signature	W. TREAT	Date Considered	3/3/07
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WMT	C2	Gulati, M. and Bagherzadeh, N., "Performance Study of a Multithreaded Superscalar Microprocessor," 2 <sup>nd</sup> International Symposium on High-Performance Computer Architecture, February 1996, 11 pages.	
	C3	Loikkanen, M. and Bagherzadeh, N., "A Fine-Grain Multithreading Superscalar Architecture," Proc. 1996 Confer. Parallel Architectures and Compilation Techniques, October 1996, 6 pages.	
	C4	Tullsen, D. M. et al., "Exploiting Choice: Instruction Fetch and Issue on an Implementable Simultaneous Multithreading Processor," Proc. Of the 23 <sup>rd</sup> ISCA, May 1996, 12 pages.	
↓	C5	Tullsen, D. M. et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proc. Of the 22 <sup>nd</sup> ISCA, June 1995, 12 pages.	
WMT	C6	Yamamoto, W., "An Analysis of Multistreamed, Superscalar Processor Architectures," Ph.D. Thesis, U.C. Santa Barbara, Dec. 1995, pp. 1-155.	

Examiner Signature	W. TREAT	Date Considered	3/3/67
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